

WHAT IS CLAIMED IS:

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1. An information processing device comprising:

an $m \times n$ (m-row x n-column) instruction buffer;

10 a plurality of instruction executing parts executing a plurality of instructions in parallel; and

a control circuit selecting a predetermined number of instructions from said $m \times n$ instruction buffer and distributing said
15 instructions to said instruction executing parts.

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2. The information processing device as claimed in claim 1, wherein said control circuit comprises n selection circuits, each of said selection circuits selecting an instruction from m
25 instructions of the corresponding column.

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3. The information processing device as claimed in claim 1, wherein said control circuit comprises n selection circuits and a control part controlling said selection circuits, said control part controlling said selection circuits by
35 referring to information included in each instruction indicating whether the instruction is simultaneously executable so as to select an

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a $1 \times n$ (1-row x n-column) buffer holding a predetermined number of instructions selected by said first selection circuits; and

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one predetermined condition.

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7. The information processing device as claimed in claim 6, wherein said predetermined instructions include conditions related to a length of instruction or a combination of instructions.

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8. The information processing device as claimed in claim 1, wherein said instruction executing part includes a plurality of slots and said control circuit includes n first selection circuits and a $1 \times n$ (1-row x n-column) buffer holding a predetermined number of instructions selected by said first selection circuits, and wherein the number of said plurality of slots being greater than or equal to the number of said $1 \times n$ (1-row x n-column) buffers holding n instructions.

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9. The information processing device as claimed in claim 1, wherein said $m \times n$ instruction buffer receives a group of instructions read out from a memory which does not include any NOP instruction.

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5 wherein said processor includes;
an $m \times n$ (m-row x n-column) instruction
buffer;
a plurality of instruction executing parts
executing a plurality of instructions in parallel;
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a control circuit selecting a
predetermined number of instructions from said $m \times n$
instruction buffer and distributing said
instructions to said instruction executing parts.

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